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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/827,056	LIU ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Wolf ("Silicon Processing for the VLSI Era : Vol.2" Lattice Press, Sunset Beach, Ca., (1990), pp. 321 – 322).

4. Regarding Claim 1, Lin et al. clearly disclose a method for forming split-gate flash memories with improved, increased coupling ratio. A common source region is formed (125) (Figure 2G) in a silicon substrate. Source implantation is done using n-type implants (Col. 6, lines 42 – 45) and drains (120) implanted at opposite sides of the source (and within the vicinity (second extremity) of gate regions) (Figure 2G) using n-type implants (Col. 7, lines 14 – 18). Floating gates (140) (Figure 2D) are formed, overlying areas of the common source region (Figure 2G) and extremities extending over the (first) part of the structure. Adjustment of channel threshold voltage using ion implantation has been used since the early 1970's and is well documented in the art (See for example, Wolf, pp.321 – 322), as is also admitted by

Applicant (page 6, line 31 through page 7, line 4) in the instant application, where it is acknowledged that it is "generally understood by those of ordinary skill in the art of semiconductor manufacturing [that] additional ion implantation processes may be necessary to adequately adjust threshold voltages."

Hence, it would be notoriously obvious to one of ordinary skill in the art to utilize ion implantation to adjust threshold voltage.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68)

Lin et al. disclose (Col. 6, lines 26 – 32) the formation of common source regions using photoresist and patterning, followed by ion implantation. Subsequent to implantation, the patterned photoresist layer is removed. Although Lin et al. disclose (Col. 6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can be readily calculated and implant conditions altered accordingly. Since the phosphorus diffuses slightly faster than arsenic (page 68), it would be desirable to use arsenic and therefore obvious to one of ordinary skill in the art at the time of the invention since both would produce similar results and thus to combine Sze, Wolf and Lin et al. to obtain ion implanted n-type impurities within a flash memory device to form source regions.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above, and further in view of Wolf et al. ("Silicon

Processing for the VLSI Era: Volume 1 – Process Technology," Lattice Press, Sunset Beach, CA (1986), pp.321 – 322).

As discussed earlier, Lin et al. disclose the the use of patterned photoresist on nitride for ion implantation masking, followed by removal of the nitride and photo-resist from the surface of the substrate. Although the use of sacrificial oxides is not disclosed, thin oxide layers are routinely used as blocking (or screening) layers for ion implants (Wolf et al., pp. 321 – 322). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wolf et al. with Lin et al. and Wolf to obtain a screening or blocking layer for the implant.

7. Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 1 above.

8. Regarding Claim 5, Lin et al. disclose (Col. 5, lines 34 – 67, Col. 6, lines 1 – 25) the formation of a thin (tunneling) oxide (130) (Figure 2B) followed by a polysilicon layer (140), and nitride (143) layer. Patterning and etching are then done to form first and second floating gate regions (Figure 2G). The overlying portion into the common source region (Figure 2G) increases the coupling ratio (Col. 7, lines 1 – 4).

As discussed earlier, threshold implant adjusts using ion implantation are routinely done in the art (Wolf, pp. 321 – 322) and it would be obvious to one of ordinary skill in the art to utilize this procedure to obtain a working device.

9. Regarding Claim 9, Lin et al. do not disclose the implantation of boron ions for threshold adjustments. The use of boron ions would be an obvious modification to Lin et al.,

since boron ions are routinely used in the industry for p-type implants and threshold adjusts (Wolf, pp. 321 – 322) in n-type regions.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 5 above.

As previously discussed, select gates are formed (Figure 2G) using patterned removal of insulating layer, second polysilicon layer overlying floating gate. Lin et al. do not explicitly identify a conductive layer. Conductive metal layers are well known in the art and it would be obvious to one of ordinary skill in the art to add to Lin et al. to include a specific conductive metal layer to complete a working device.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6 above, and further in view of Mizuno et al. ("Hot Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure," IEEE Trans. on Electron Devices, Vol.38, No. 3, (1991), pp. 584 – 591).

An oxide layer (170) overlies the first oxide, floating gate oxide (145) (See Figure 2G) and spacers at the lateral edges of gates. Lin et al. do not disclose the composition of the spacer as a nitride. However, the use of nitride spacers is notoriously well known in the art and Mizuno et al. disclose the use of nitride spacers on gate structure for improved device performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the nitride spacers of Mizuno et al in Lin et al. and to combine Mizuno et al. with Wolf and Lin et al. to obtain appropriate hot carrier suppression.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 6, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ.,Westwood, New Jersey, (1993), p. 868).

Lin et al. do not disclose a tungsten conductive layer. Tungsten, however, has been routinely utilized in the art (Wilson et al., page 868, 1st paragraph) for plugs, inter-connects, and standard metallization levels. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize Wilson et al. in forming tungsten conducting layers to obtain stable contacts, and to combine Wilson et al. with Wolf and Lin et al.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., in view of Wolf, as applied to Claim 6 above. Lin et al.disclose (Col. 7, lines 14 – 18) the formation of ion implanted drain regions, but do not explicitly teach the patterning and etching of a conducting film. As discussed earlier, it would have been obvious to add a conducting film layer to complete the device.

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., in view of Wolf and further in view of Wolf et al., as applied to Claim 4 above.

Lin et al. (Col. 6, lines 42 – 45) disclose the use of a phosphorus implant for forming the common source region, whereas, the instant application recites the use of an arsenic ion implant. However, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can be readily

calculated and implant conditions altered accordingly. Since the phosphorus diffuses slightly faster than arsenic (page 68) , it would be desirable and therefore obvious to one of ordinary skill in the art at the time of the invention to use arsenic since both would produce similar results and thus, to combine Sze, Wolf and Lin et al. to obtain ion implanted n-type impurities within a flash memory device to form source regions.

15. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, as applied to Claim 5 above.

Lin et al.disclose the formation of a polysilicon layer using LPCVD with a SiH4 source at a temperature of 550 to 600 degrees (C) to thickness between about 1500 to 2500 Angstroms (Col. 6, lines 58 – 62). These are in the range of values recited in the instant application. It has been held that where a general condition of a claim is disclosed in prior art, discovering the optimal or workable range involves only routine skill in the art.

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al.

Lin et al. clearly disclose a process (as previously discussed) for fabricating a flash memory device having a high coupling ratio, as recited in the instant application. The formation of a sacrificial oxide, although not disclosed by Lin et al. is a commonly used procedure and obvious to one of ordinary skill in the art. Patterning and etching are used to define source regions. A first ion implant is then used to form the source regions and subsequently, the photoresist layer is removed. After forming a thin tunneling oxide layer, a polysilicon layer and a nitride layer, patterning and etching are done to define floating gate regions, where threshold implants are done. Although Lin et al. do not disclose the

use of threshold implants, Wolf (page 321) discloses the use of such threshold implants as common procedure. Lin et al. disclose the formation of the floating gate structures having sidewalls with portions overlying the common source region and increasing the coupling ratio. Similarly, Lin et al. do not disclose the use of nitride spacers on gate edges, but Mizuno et al. (page 584, right side) disclose the use of nitride spacers on the lateral edges of gates to suppress hot carrier injection. An oxide layer overlies the first oxide, floating gate oxide and spacers at the lateral edges of gates. A second polysilicon layer overlies the second oxide. Patterning and etching are used to define select gates and the boundaries of drain areas. Lin et al. do not disclose the formation of a conductive layer but this would have been obvious to complete the device. Further, Wilson et al. disclose that conducting layers such as tungsten are routinely deployed in applications. Ion implants into drain regions are disclosed by Lin et al. using arsenic ions.
It would have been obvious to one of ordinary skill in the art at the time of the invention To utilize the threshold implants of Wolf, the nitride spacers of Mizuno et al. and the conductive tungsten layers of Wilson et al. to form a working device with controlled threshold voltage, reduced hot carrier effects and stable contacts and to combine Wolf, Mizuno et al., and Wilson et al. with Lin et al. to obtain a flash memory cell with increased coupling ratio.

17. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Wolf, Mizuno et al., and Wilson et al., as applied to Claim 14. It can again be noted that the use of ion implantation for adjustment of threshold volt age is a notoriously well known procedure and commonly deployed since the inception of commercial

ion implantation equipment in the industry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize ion implantation in Lin et al. for threshold voltage adjustment.

Response to Arguments

14. Applicant's arguments with respect to claims 1 – 14 and 16 in Letter No. 13 of June 2, 2003 have been considered but have been found to be unpersuasive.

With regard to Claims 1 and 14, Examiner can only interpret language posed in limitations of claims and currently, Lin et al. discloses those tenets recited in the claims of the instant application of Applicant. There is no chronology of process steps disclosed in the reference or recited in the claims of the instant application. Therefore, arguments appear moot. It should also be noted that the implantation process is clearly used to increase the coupling ratio in Lin et al.

With regard to ion implantation of phosphorus rather than arsenic, Applicant has failed to clearly show that phosphorus cannot be used or that differing coupling ratios are attained. The lateral diffusion in the reference (Figure 2G) is both calculable and useful for increasing coupling. Applicant also recognizes the contribution of extension beneath the floating gate (page 8, lines 28 – 30) "*This increased source side coupling ratio is due to the distance 202 the source region 116 extends beneath the floating gate 124A, 124B being increased...*"

Arguments pertaining to enhanced vertical diffusion of phosphorus are irrelevant here, both from the viewpoint that the thermal budget is scant, and from the results of Lin et al. who showed an increase in coupling. Applicant has been unsuccessful in demonstrating otherwise.

Conclusions

15. Any inquiry concerning this communication should be addressed to **Thomas Magee**, whose telephone number is **(703) 305- 5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM. If attempts to reach the Examiner by phone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772**. The appropriate fax phone number for the organization where this application or proceeding is assigned is **(703) 308-0956**.

Tom Thomas

TOM THOMAS
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Thomas Magee
June 12, 2003